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The role of H in the Cu^+ drift diffusion in plasma-deposited a-SiC:H

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Abstract

Advanced back-end processing of integrated circuits requires the integration of low-k dielectrics and Cu. Plasma-deposited films for hard-mask use with good resistance to wet chemicals, aggressive etching, and chemical mechanical polishing are essential for a successful integration of these materials. As a solution to the problem of how to provide quality hard masks, a process has been developed for deposition of a trimethylsilane-based a-SiC:H. Depending on the deposition temperature and additional thermal treatments, the dielectric constant, k, can be varied between 4.2 and 5.8. Thermal stability of the a-SiC:H up to 500 °C was found. Decreasing hydrogen content in the film is found for increasing k-value. The Cu^+ drift rate in the different types of a-SiC:H is quantified using bias temperature stressing in combination with high-frequency capacitance/voltage (C/V) measurements on capacitor structures. The drift diffusion experiments indicate that the Cu^+ drift rate in the film is retarded with increasing k-value for the a-SiC:H, which is attributed to a reducing hydrogen content and a densification of the film. Moreover, a-SiC:H is a potential candidate for replacing the high-dielectric-constant Si_3N_4 as a Cu diffusion barrier and hard mask.

1. Introduction

Damascene architectures incorporating organic and porous low-k materials require an inorganic dielectric liner when used as the hard mask for dielectric capping layers, antireflective coating or a polishing stop with good resistance to aggressive etching, stripping, and chemical mechanical polishing processing [1]. In addition, these inorganic dielectrics should show excellent barrier behaviour against Cu diffusion. For standard Cu dual damascene processing, Si_3N_4 is mainly used as the hard-mask material [2]. It is known that plasma-deposited Si_3N_4 acts as a Cu^+ drift

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barrier, whereas plasma-deposited silicon dioxide does not [3,4]. At process temperatures for back-end integration (<450 °C), thermal diffusion of Cu into oxide is negligible [5]. However, in the presence of an electrical field, positive Cu ions can drift rapidly through oxide, causing reliability problems [5,6]. Thermodynamic calculations show that mainly Cu^+, as opposed to atomic neutral Cu, is injected into the dielectric during stressing [7].

The high dielectric constant k of Si_3N_4 ($k \approx 8$) motivates the development and use of other plasma-enhanced chemical vapour deposition (PECVD) materials. The most promising candidate for replacing Si_3N_4 is a-SiC:H because of its low dielectric constant ($4.2 < k < 4.9$). It is an amorphous material and can be deposited in a CVD system. In this work, the role of hydrogen in the a-SiC:H with respect to Cu^+ drift diffusion is investigated. These results on the drift diffusion are also compared with those obtained from a traditional PECVD Si_3N_4 and oxide.

Conventional characterization techniques, including Rutherford backscattering spectroscopy (RBS), secondary-ion mass spectroscopy (SIMS), and Auger electron spectroscopy (AES) have been used to investigate Cu^+ drift diffusion. However, most of these techniques lack high sensitivity as well as direct applicability to electrical performance [1]. Electrical characterization provides higher sensitivity for quantifying the drift diffusion. In back-end processing, biased temperature stressing (BTS) of metal/insulator/silicon structures using metal contacts to the dielectric provides both a practical and sensitive electrical technique through flat-band voltage shifts (ΔV_{FB}). In this technique, a voltage is applied across the capacitor, which is simultaneously being annealed at high temperatures, and the resulting effects on the capacitance/voltage (C/V) behaviour are subsequently measured at room temperature [8]. As already mentioned above, the flat-band voltage V_{FB} is an important parameter in investigating the drift diffusion and is defined as

$$V_{FB} = \phi_{ms} - \frac{Q_i + Q_{it}}{C_{max}}. \tag{1}$$

C_{max} is the accumulation capacitance per unit area and ϕ_{ms} is the difference in work-function between the metal gate and Si. Q_{it} is the interface trapped charge and Q_i is the equivalent interfacial dielectric charge at the dielectric/Si interface [8]. Q_i is a sheet charge located near the dielectric/Si interface containing the same amount of charge per unit area as in the dielectric and includes fixed charge, mobile charge, and trapped charge present in the dielectric. Cu ions that drift in the dielectric up to the Si/dielectric interface cause a change in Q_i (Q_{it}). This will be reflected in a lower value of V_{FB}. A sensitivity to a level of migrated metal atoms as low as 2.2×10^{10} atoms cm^{-2} is obtainable from the C/V response [1]. In this paper, the BTS technique combined with C/V measurements were used to investigate the Cu^+ drift diffusion in the a-SiC:H and Si_3N_4 layers.

2. Experimental details

Typical metal–insulator–silicon capacitor test structures were fabricated using ⟨100⟩ n-type silicon substrates (figure 1). A layer of 60 nm thermal oxide was grown on the Si substrate; this was followed by the deposition of a thin conformal a-SiC:H or Si_3N_4 layer with a thickness that varied between 10 and 50 nm. Cross sectional TEM pictures were also used to determine the thickness. To obtain the standard a-SiC:H with a dielectric constant around 4.9, the deposition was done at 400 °C. The dielectric constant decreased to 4.2 if the layer was deposited at 350 °C. The Si_3N_4 was deposited at 400 °C and has a dielectric constant around 8. Cu was sputtered on top of the dielectric using a shadow-mask. The shadow-mask was used to obtain a circular metal gate with an area of approximately 2.2 mm^2. To avoid severe oxidation of the

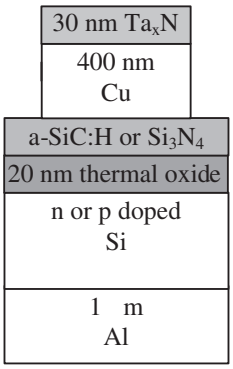


Figure 1. The experimental capacitor structure used to investigate Cu^+ diffusion in a-SiC:H and Si_3N_4.

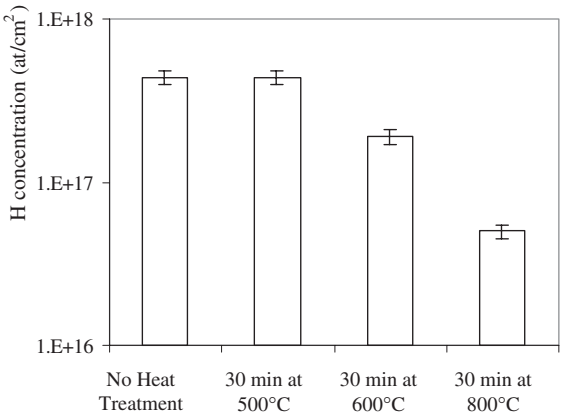


Figure 2. Hydrogen concentration in 100 nm a-SiC:H films deposited at 400 °C versus different heat treatment temperatures (for 30 min in N_2) as measured using ERD. All films received an initial heat treatment under H_2/N_2 for 10 min at 400 °C.

Cu metal during BTS, 30 nm of Ta_xN was deposited on the Cu. Al metal gate capacitors were processed in the same way and used as a reference. Al back-face sputtering was necessary to provide a good electrical contact during the measurement. Prior to electrical measurements all the capacitor structures received an initial heat treatment of 10 min at 400 °C in N_2/H_2. The thermal treatment annealed out the sputter damage, to give a well-behaved C/V curve [9].

Some a-SiC:H samples deposited using the 400 °C process were additionally heat treated for 30 min up to 800 °C. Minor changes ($\Delta V_{FB} < 0.1$ V) in the C/V characteristics were seen after the heat treatments, indicating no detectable evidence of thermal Cu diffusion in the dielectric film. Elastic recoil detection (ERD) demonstrates no decrease of the hydrogen concentration in a 100 nm a-SiC:H film up to 500 °C (figure 2). This is confirmed using infrared spectroscopy where the spectra remain unchanged. Heat treatments above this temperature lead to a significant decrease of the hydrogen content. Thickness measurements of the a-SiC:H film, using TEM cross sections, show a decrease of the thickness for the thermally treated samples above 500 °C. A densification of the dielectric of around 10 and 15% was seen for the samples heat treated at 600 and 800 °C, respectively. Using C_{max} and d, the dielectric layer thickness (obtained from TEM cross sections), the dielectric constant k can be calculated

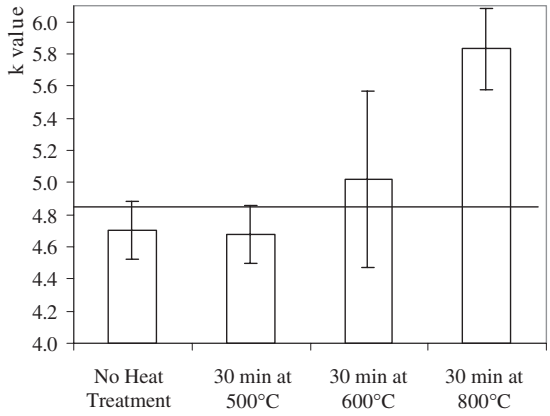


Figure 3. Dielectric constant k of the a-SiC:H film deposited at 400 °C versus different heat treatments (for 30 min under N_2). All films received an initial heat treatment in H_2/N_2 for 10 min at 400 °C.

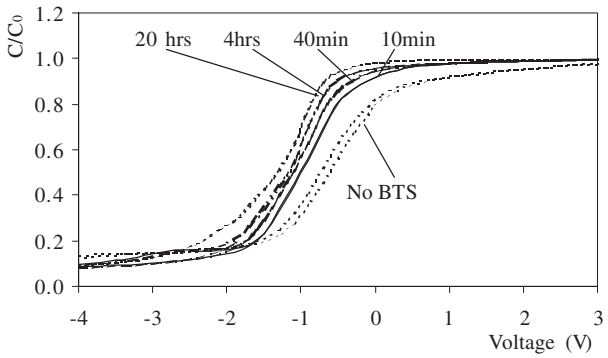


Figure 4. Normalized C/V curves of a 10 nm a-SiC:H ($k \approx 4.8$) capacitor structure with a Cu gate for different BTS times (2.8 MV cm^{-1} at 275 °C); C_0 is the accumulation capacitance.

using equation (2). ε_0 is the permittivity of vacuum and equals 8.85×10^{-12} A s V^{-1} m^{-1}. Figure 3 shows that a densification of the film results in a higher dielectric constant—mainly for the samples heat treated at 800 °C. The hydrogen content in a 100 nm film of a-SiC:H deposited at 350 °C without any additional heat treatment (9×10^{18} atoms cm^{-2}) was higher than in a film deposited at 400 °C (5×10^{17} atoms cm^{-2}). These results show that a higher amount of H in the a-SiC:H film results in a lower k-value. We have

$$C_{max} = \frac{k\varepsilon_0}{d}. \tag{2}$$

C/V measurements in combination with BTS were used to study the Cu^+ drift diffusion. The electrical field was varied between 1 and 2.8 MV cm^{-1} with a stressing time up to 20 h (200–300 °C).

3. Results and discussion

Typical C/V curves of a 10 nm a-SiC:H capacitor for different stressing times when applying a positive field of 2.8 MV cm^{-1} are shown in figure 4. Increasing stressing time causes a

Table 1. Estimates of the initial flat-band voltage shift ΔV_{FB} for positively biased Cu or Al/10 nm hard-mask material/60 nm thermal oxide/Si capacitors after 10 min of stressing.

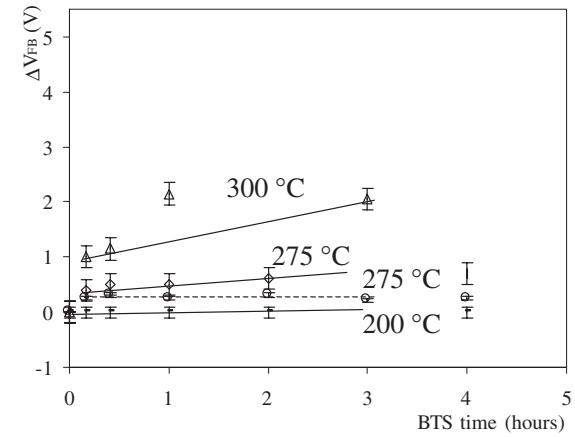
Hard mask material:	a-SiC:H (400 °C)		a-SiC:H (400 °C) + 30 min/800 °C/N_2	a-SiC:H (350 °C)	Si_3N_4
Gate bias:					
BTS temperature (°C)	+	−	+	+	+
200	0.0 ± 0.1	0.0 ± 0.1	0.0 ± 0.1	0.0 ± 0.1	0.0 ± 0.1
275	0.3 ± 0.1	-0.1 ± 0.1	0.1 ± 0.1	0.4 ± 0.1	1.9 ± 0.1
300	0.8 ± 0.1	-0.6 ± 0.1	0.3 ± 0.1	1.1 ± 0.1	3.9 ± 0.1

larger shift towards the left of the C/V curve. However, no pronounced spreading out of the C/V curve (except for the 20 h C/V curve) is observed, indicating that the number of interface states remains unchanged. Moreover, after a short initial stressing (≈10 min), a reduction of the C/V spreading indicates a decrease in the number of interface traps. The same behaviour is also observed for Si_3N_4 capacitors. Figure 5 shows the flat-band voltage shift ΔV_{FB} as a function of BTS stressing time for both a-SiC:H and Si_3N_4 capacitors with Cu and Al gates. Each datum point is an average from at least three tested capacitors and ΔV_{FB} is defined as expressed in equation (3). A lower value of the V_{FB} after BTS (e.g. due to an increase of Cu^+ in the dielectric) results in a positive ΔV_{FB}:

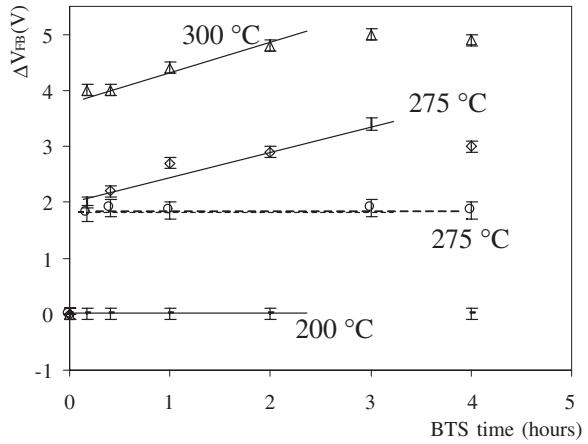
$$\Delta V_{FB} = V_{FB} \text{ (before BTS)} - V_{FB} \text{ (after BTS)}. \tag{3}$$

A rapid initial change of ΔV_{FB} is observed when applying a positive bias for both Al and Cu gate capacitors. Table 1 gives an overview of the initial shift for the different hard-mask materials under study. This shift is more pronounced for stressing at higher temperatures and fields. Exposing the a-SiC:H to a heat treatment at 800 °C reduces the effect. The Al gate capacitors show saturation after this initial shift, whereas the Cu gate capacitors keep on increasing for longer stressing times (figure 5). Another observation is that the initial change is larger for Si_3N_4 than for a-SiC:H-containing capacitors. Since the rapid initial shift is present for both Al and Cu gate capacitors, it could be attributed to the movement of mainly trace alkali impurities or other contaminants in the dielectric originating from the metal gate electrode during deposition [10]. The effect of the fast-moving alkali ions, such as Na^+, saturates when the limited ions accumulate at the Si substrate interface. The subsequent increase in ΔV_{FB} for the Cu capacitors is due to the slower Cu ions that are injected by the Cu gate. In addition, Fang *et al* [11] and Gritsenko *et al* [12] suggest that these shifts are also due to a molecular polarization in the carbide or nitride film. This polarization contributes to the electrical dipole orientation in the film and induces a charge in the silicon substrate, which is reflected by a shift in the C/V curve. A negative ΔV_{FB}—but less pronounced than for a positive bias—is seen when a negative bias is applied (table 1). A similar behaviour is observed for both the Al and Cu gate capacitors: a rapid initial ΔV_{FB} that remained constant for longer stressing times. These assessments verify the postulation of polarization in the film. The chemical bonds that are mainly responsible for the polarization are Si–N, Si–NH_x, and hydrogen bonds [2]. This results in the higher initial shifts for Si_3N_4 than for a-SiC:H as shown in figure 5 and table 1. Moreover, the lower the amount of hydrogen in the a-SiC:H film, the lower the shift.

The continuous increase in ΔV_{FB} for positively biased Cu capacitors as opposed to Al gate capacitors (figure 5) is due to the injection of Cu ions from the Cu gate. The constant ΔV_{FB} for Cu and Al capacitors when applying a negative field verifies the Cu-ion polarity. Capacitors with a thickness of the hard-mask layer above 10 nm give no indication of ionic Cu-related diffusion. For all conditions tested, unbiased Cu and Al gate capacitors with a



(a)



(b)

Figure 5. Flat-band voltage shift ΔV_{FB} versus BTS time and temperature for 10 nm a-SiC:H ($k \approx 4.8$) (*a*) and Si_3N_4 (*b*) capacitors with a Cu gate ($E = 2.8$ MV cm^{-1}). A dashed line relates to capacitors with an Al gate.

10 nm hard-mask layer show a negligible shift of V_{FB} ($\leqslant$0.05 V) within the test window (20 h, 200–300 °C), indicating no detectable thermal diffusion. Performing SIMS measurements on the tested hard-mask materials was not possible since interface effects masked the complete Cu diffusion profile for the layer. RBS and AES are not sensitive enough.

In order to quantify the diffusion, the initial drift rate of Cu ions in the 10 nm layers is calculated using equation (4), where q is the electronic charge. The equation assumes that the Cu ions have drifted to the oxide–substrate interface. The initial drift rate is determined since the electrical field in the dielectric changes with time due to accumulation of Cu ions [6]. In order to solve this equation, the slopes of best-fit lines through the different ΔV_{FB} data points versus stressing time were calculated (figure 5). By using the slopes, the effect of the rapid initial increase of ΔV_{FB}—which is not correlated with Cu^+ drift diffusion—is ignored.

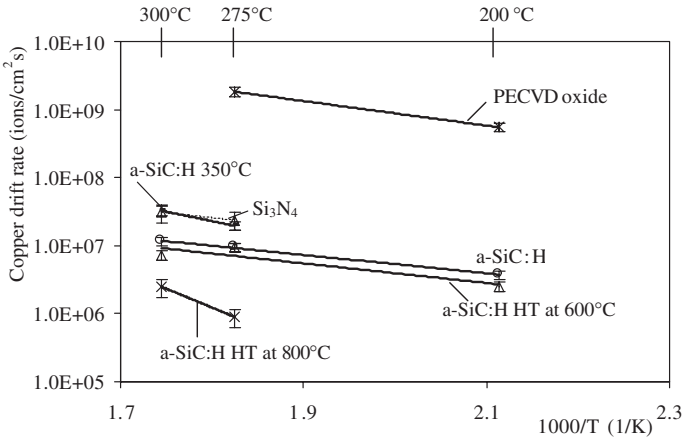


Figure 6. An Arrhenius plot of the initial Cu^+ drift rate in a-SiC:H deposited at 400 °C that received different heat treatments (HT), for 30 min in N_2. The Cu^+ drift rate in a film deposited at 350 °C is plotted as well. The dashed lines give results for PECVD oxide and Si_3N_4. The drift rate is determined at an applied electrical field of 2.8 MV cm^{-1}.

Arrhenius plots of the drift rates for three different types of a-SiC:H are shown in figure 6. We have

$$[Cu^+] = -\frac{C_{max}}{q}\frac{\mathrm{d}}{\mathrm{d}t}(\Delta V_{FB}). \tag{4}$$

Capacitors stressed at 1 MV cm^{-1} did not show any evidence of Cu^+ drift diffusion for any type of a-SiC:H or Si_3N_4 and therefore it was not possible to calculate the Cu^+ drift rate at this field. The a-SiC:H processed at 350 °C has a slightly higher drift rate as compared to the one processed at 400 °C. a-SiC:H deposited at 400 °C and additionally heat treated at temperatures higher than 500 °C tends to have a retarded Cu^+ drift rate as compared to the non-heat-treated layers. It is only the heat treatment at 800 °C that causes a significant decrease of the drift rate. These findings, in combination with the results shown in figure 2, suggest that a lower amount of hydrogen in the a-SiC:H results in a lower drift rate. As confirmed by the thickness measurements on the a-SiC:H film, a lower drift rate is probably caused by a denser structure of the material, which is reflected in a higher value of the dielectric constant (figure 3). A comparison of the initial Cu^+ drift rate in a-SiC:H with those for Si_3N_4 and PECVD oxide is included in figure 6 as well. The Cu^+ drift diffusion in PECVD oxide was evaluated using Si/20 nm thermal oxide/100 nm PECVD oxide/Cu capacitors [13]. Both a-SiC:H and Si_3N_4 perform better than PECVD oxide. Moreover, the a-SiC:H film is even more resistant to Cu^+ drift diffusion than Si_3N_4. Taking the additional advantage of a lower dielectric constant into account, a-SiC:H becomes a potential candidate for replacing Si_3N_4 as a hard-mask material.

The estimated initial drift mobility μ of Cu^+ in the different dielectrics investigated, as a function of temperature, is presented in figure 7. Every datum point is an average over experiments done at three different values of the electrical field, and at least three capacitors were evaluated for each value of the electrical field. The actual calculation is performed using equation (5), where d_{ox} and d_{diel} are the thicknesses of the thermal oxide and dielectric, respectively, E is the electrical field, and μ^{ox} is the initial Cu^+ drift mobility in thermal oxide [5]:

$$t_{drift} = t^{ox}_{drift} + t^{diel}_{drift} = \frac{d_{ox}}{\mu^{ox}E} + \frac{d_{diel}}{\mu E}. \tag{5}$$

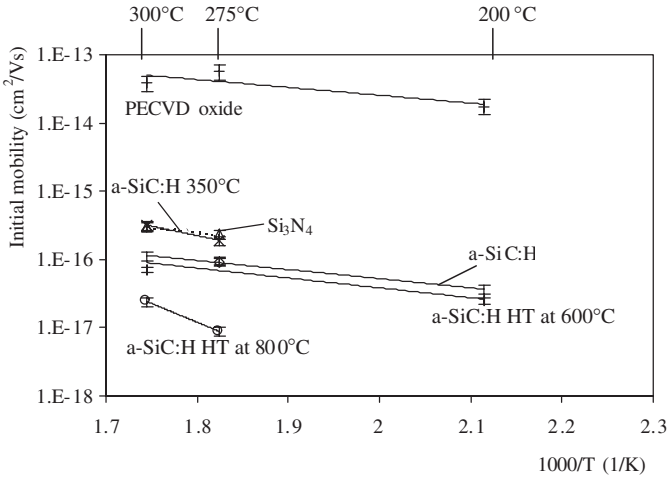


Figure 7. Initial mobility of Cu^+ in differently processed a-SiC:H materials and Si_3N_4. PECVD oxide is given as a reference; HT stands for heat treatment.

The total drift time, t_{drift}, is defined as the time required to diffuse 2.2×10^{10} atoms cm^{-2} (Cu ions) through the dielectric (t^{diel}_{drift}) and the thermal oxide (t^{ox}_{drift}) up to the Si/thermal oxide interface. t_{drift} is the approximate time required to observe a ΔV_{FB} of 0.1 V in the measured C/V curves due to Cu diffusion [5]. Indeed, this shift corresponds to a concentration of approximately 2.2×10^{10} atoms cm^{-2} for the Cu ions in the dielectric near the dielectric/Si interface. The reason that these charges are present near the Si/dielectric interface rather than distributed in the dielectric is related to the C/V method. This technique is more sensitive for charges near the Si/thermal oxide than for ones near the thermal oxide/gate interface [13, 14].

However, in addition to shifts in the V_{FB} due to Cu^+ diffusion, a constant shift that is not related to Cu^+ diffusion is seen. Therefore t_{drift} is defined as the time at which ΔV_{FB} equals the sum of the constant shift and 0.1 V and is determined by interpolating the experimental data points shown in figure 5. Since μ^{ox}_{Cu} in thermal oxide is extracted from BTS and C/V using a Si/20 nm thermal oxide/Cu capacitor, μ can be calculated [10]. Also here the initial mobility is calculated, since the electrical field in the dielectric changes over time due to accumulation of Cu^+ ions.

Since the calculation of μ is also based on the C/V results, the same conclusions as for the Cu^+ drift rate are valid. An overview of the calculated activation energies for both the drift rate and the mobility is presented in table 2. The activation energy for Cu^+ drift diffusion can be derived from the Arrhenius plots of figures 6 and 7 [10]. In addition, the accumulated Cu ions in the dielectric, after 10 years of operation at 100 °C and 2.8 MV cm^{-1}, are also calculated in table 2. The activation energies for the a-SiC:H samples that were subsequently heat treated above 500 °C are not included, since such heat treatments cannot be allowed in a typical Cu/low-k back-end process (temperature <450 °C). A good agreement is seen between the calculated activation energies for the different methods. PECVD oxide, Si_3N_4, and a-SiC:H (deposited at 400 °C) show similar activation energies, indicating comparable diffusion mechanisms. In contrast, a-SiC:H deposited at 350 °C demonstrates a higher activation energy, which is probably related to the fact that the Arrhenius fitting is done through data points at two different temperatures. This higher activation energy explains also the lower accumulated level of Cu^+ ions for the a-SiC:H deposited at 350 °C than for that deposited at

Table 2. Activation energy as calculated from the Cu^+ drift rate at 2.8 MV cm^{-1} and mobility in a-SiC:H, Si_3N_4, PECVD oxide and accumulated levels of Cu^+ ions in the dielectrics after 10 years of operation at 2.8 MV cm^{-1} and 100 °C.

	Activation energy (eV)		Accumulated Cu^+ (ions cm^{-2})
Calculated from	Drift rate	Mobility	Drift rate
a-SiC:H deposited at 400 °C	0.27 ± 0.09	0.29 ± 0.09	2.1×10^{14}
a-SiC:H deposited at 350 °C	0.55 ± 0.09	0.56 ± 0.06	5.3×10^{13}
Si_3N_4	0.29 ± 0.09	0.29 ± 0.06	4.3×10^{14}
PECVD oxide	0.36 ± 0.09	0.30 ± 0.06	1.8×10^{16}

400 °C after 10 years of operation at 2.8 MV cm^{-1}. Even though the working conditions are more stringent than are required for an integrated circuit (2.8 MV cm^{-1} instead of maximum 1 MV cm^{-1}), the carbide and nitride hard-mask materials show a significant improvement over PECVD oxide as regards the accumulated Cu ions. The accumulated ion levels in PECVD oxide are at least two orders of magnitude larger than in the hard-mask films. As expected, the numbers of accumulated ions at working conditions for a-SiC:H and Si_3N_4 are comparable.

4. Conclusions

The ionic Cu drift diffusion in 10 nm of trimethylsilane-based a-SiC:H ($4.2 < k < 4.9$) is investigated by means of BTS and C/V measurements. The a-SiC:H is proven to be a potential candidate for replacing the high-dielectric-constant Si_3N_4 as a Cu diffusion barrier and hard-mask material. The drift diffusion rate can be retarded by an additional heat treatment of the a-SiC:H above 500 °C. ERD, and thickness measurements of the a-SiC:H layers reveal that the decrease in Cu^+ drift diffusion rate can be attributed to a lowering of the H content in the film that corresponds to an increase in film density. Both Si_3N_4 and a-SiC:H are effective dielectric Cu^+ barriers as compared to PECVD oxide. An even better performance is expected for thicker hard-mask layers since no diffusion could be detected if the thickness exceeded 10 nm. This indicates that the barrier properties degrade for thinner layers. However, the hard-mask thickness must be minimized to preserve the low-k advantage of the inter-level dielectric without compromising barrier integrity.

Acknowledgments

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